8-bit Arithmetic Logic Unit Design Report

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2007-12-09
8bit ALU Design Report

Outline
- Generalization
- Function
- Structure
- Assignment
- Design results
- Summary
ALU (Arithmetic Logic Unit)

A critical component of the microprocessor, the core component of central processing unit. ALU comprises the combinational logic that implements logic operations such as AND and OR, and arithmetic operations such as Addition, Subtraction, and Multiplication.
Generalization

A and B: N-bit Inputs
Result: N-bit Output
Op: ALU operation, K-bit means could support maximum $2^k$ operation
Zero, CarryOut, Overflow: 1-bit flag

ALU symbol

A \rightarrow N \quad \text{Op} \quad K \quad \text{B} \rightarrow N

ALU

\text{Result}

\text{CarryOut}

\text{Zero}

\text{Overflow}
8 Functions

LOGIC: And; Or; Inv

SHIFT: signed-shift left
      signed-shift right

ALGORITHM: Add
           Subtract
           Multiply

3 bit control signals

To choose the function
Structure

Schematic – 7 components
Structure

Layout - place
Assignment

- Logic & Control – Wei Zhong
- Shift – Yang Zhao
- Add & Subtract – Hongxia Fang
- Multiply – Zhaobo Zhang

Everyone is in charge of each part's schematic simulation and layout verification
Design results

8 to 1 MUX
- Using compound gate to realize 2 to 1 MUX

\[ Y = D \cdot \overline{S} + D \cdot S \]
8 to 1 Mux
Set A0=1, A1~A7=0.
when S2S1S0=000, Out=1
8-bit 8 to 1 Mux
Layout of 1-bit Mux81

2-bit Mux81
Logic Function

- 8-bit AND
Simulation for 8bit input AND

Logic Function

8bit OR
Simulation for 8bit input OR

Simulation for 8bit input AND & OR
Logic Function

8bit Inverter
Simulation for 8bit input OR

Input A[7:0]=01010101, Q[7:0]=10101010
Signed-Shift Right Schematic
Simulation for Signed-shift right

$S_0S_1S_2=010$, connect $A_0$ to extra bit, shift $A_7\sim A_0=00101011$ right for 2 bits, the output $R_7\sim R_0=11001010$
Signed-shift right Layout

consist of 24 2-input MUX, using Metal 1 and Metal 2 interconnects
Signed-shift left  
Schematic
Simulation for Signed-shift left

$S_0S_1S_2=010$, connect A7 to extra bit, shift A7~A0=00101011 left for 2 bits, the output R7~R0=10101100
Signed-shift left Layout

consist of 24 2-input MUX, using Metal 1 and Metal 2 interconnects
8-bit ripple Adder schematic
8-bit ripple Add-sub schematic
Simulation
1-bit full adder layout
8-bit ripple adder layout (part)
8-bit add-sub layout (part)
4-bit Booth Multiplier

Schematic
4-bit Booth Multiplier

Simulation

\[ B \times A = 2 \times 3 \]

Multiplier A \[\quad \text{---0000 0011}\]
Multiplicand B \[\quad \text{---0010 0000}\]

Stage 1: \[0000 001\text{10}\] subtract B, shift
- \[0010 0000\]

Stage 2: \[1111 000\text{11}\] nothing, shift

Stage 3: \[1111 100\text{01}\] add B, shift
+ \[0010 0000\]

Stage 4: \[0000 1100\text{00}\] nothing, shift

Product: \[0000 0110\]-----done, \(6 = 2 \times 3\)
4-bit Booth Multiplier

Stage 1 output: 11110001
Stage 2 output: 11111000
Stage 3 output: 00001100
Stage 4 output: 00000110
4-bit Booth Multiplier

Layout
Summary

- We successfully design 8-bit ALU, supporting 4-bit multiplication.
- The design has a right simulation result and passes the DRC and LVS verification.
- Final chip:
  - 4464 transistors
  - $S=2\text{mm} \times 2\text{mm}$