# Semi-empirical SPICE Models for Carbon Nanotube FET Logic

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***Abstract* — To evaluate the potential of carbon nanotube field effect transistors (CNFETs) to replace silicon CMOS technology, we develop a SPICE model of CNFET nanoelectronics. Our model is parameterizable, and it enables composition of models of various aspects of nanoelectronic behavior. Comparing CNFET nanoelectronics against current CMOS technology and future projections for CMOS, we demonstrate that CNFET nanoelectronics can achieve significantly greater performance at a fraction of the switching energy.**

***Index Terms* — Nanotechnology, carbon nanotubes.**

## I. Introduction

Recent research in nanoelectronics has begun to explore the potential of carbon nanotube field effect transistors (CNFETs) as a successor to CMOS. Studies of individual carbon nanotubes [13] have demonstrated that they have excellent electrical properties, including high electron mobility. Experiments with CNFETs [16, 6, 17] have further demonstrated that these devices have large transconductances, which indicates a great potential for nanoelectronic circuits. While studies of individual nanotubes and CNFETs provide reason for optimism, they are not comprehensive enough to enable conclusions about large-scale nanoelectronics. The viability of CNFET electronics depends on the behavior of logic gates that are composed of multiple CNFETs and used in larger circuits.

To discover the viability of CNFET electronics, we have developed general SPICE circuit models for this technology (Section II). For our experiments, we parameterize CNFET features (e.g., gate capacitance) based on data from published experimental results. The model then characterizes the behavior of individual CNFETs in larger ensembles of devices. Ongoing laboratory work in our research group is exploring the electronic properties of carbon nanotubes, and we will parameterize our model with this data when it becomes available. Previous work has shown how to model 2-terminal devices, and it relies on parameter fitting and device behavior decomposition [14, 7]. Our simulation methodology can model 3-terminal devices with analytical parasitics for AC response, and use a high-fidelity representation of the actual device. Thus our simulation model is a versatile and powerful tool for analyzing nanoelectronic circuits.

We use the SPICE simulations to experiment with our CNFET circuit model and explore its behavior on a variety of fundamental electronic circuits (Section III). These circuits include logic gates (inverters, NAND, NOR), combinational logic circuits (full adder), and an SR latch. We then compare CNFET behavior—in terms of switching delay and energy consumption—against SPICE simulations of a range of CMOS technology nodes. We simulate current and future CMOS technologies, as predicted by the ITRS roadmap [9], to enable fairer comparisons. Our results show that, even for optimistic future CMOS technologies, CNFET electronics offers large advantages in performance and energy.

## II. Technology and circuit models

In this section, we present our device and circuit models for both CMOS and CNFET electronics.

### A. CMOS

We use several different CMOS technology nodes for three reasons. First, by starting with well-established nearly-current technology (180nm), we provide a sound basis for extending to predictive future models. Second, using predictive models of long-term CMOS technology (45nm) enables us to provide a fair comparison for CNFET technology. Third, having multiple CMOS technologies between these extremes (some of which are still predictive [2]) allows us to observe trends. The CMOS models we use are all optimistic in that they underestimate parasitic capacitances and inductances by neglecting the bulk of interconnect between circuit nodes.

### B. CNFET Electronics

We have developed a parameterizable and composable model for CNFET electronics. The model is general and can be parameterized to fit the desired CNFET fabrication technology. For example, gate capacitances will differ based on whether the CNFETs are back-gated, electrolyte-gated, or use a metallic nanotube gate. For our experiments, we parameterize the model by composing published results from models of various CNFET features. These features include IV switching characteristics, resistances, capacitances, and inductances. We assume a car-

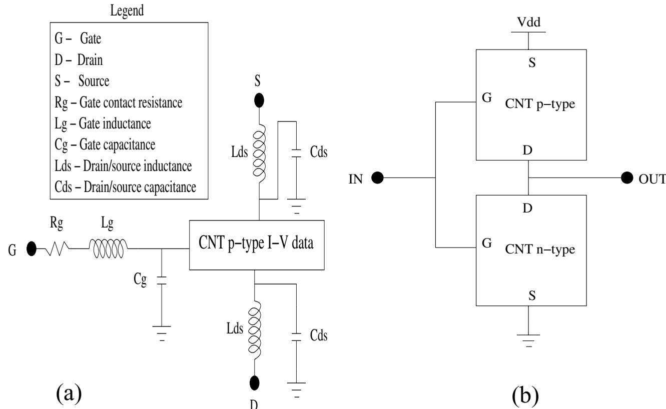


Fig. 1. Carbon nanotube (a) p-type FET and (b) inverter.

bon nanotube length of 20 nm to model an aggressive integration density. Future work will parameterize the model based on experimental results from our group.

**IV relationships.** To model the CNFET's IV characteristics, we use electrolyte-gated CNT data from Rosenblatt [15] as the empirical device data for our p-type CNFET. Our custom SPICE 3f5 kernel uses this raw data to determine branch currents within the circuit given a set of applied voltages (e.g., $V_{gs}$ and $V_{ds}$). We have created a synthetic n-type model by inverting both the $I_{ds}$ and $V_{gs}$ data from the p-type CNFET. This model is somewhat unrealistic because it does not consider the usual variation in $V_{th}$ between n-type and p-type devices, but it represents a first-effort approach to evaluating complementary electrolyte-gated CNFET circuitry. Alternatively, other device data can be used by the model including CNFETs with back or top gates [12] or crossed nanotube gates [6].

**Resistances.** The DC impedances of metallic carbon nanotubes (used to carry signals between CNFETs) in the circuit are modeled as simple lumped ohmic resistances of 6.5 k$\Omega$ per nanotube [11, 10] with a capacitance to ground ($C_{ds}$), and a series inductance ($L_g$) as described below. Contact resistances between metallic junctions and nanotubes have been modeled as lumped resistances of 25 k$\Omega$ per contact ($R_g$). This is much worse than the best possible contact resistances observed but covers worst-case process variation. These contact resistances appear at each end of a metallic carbon nanotube and on the gate of the CNFETs.

**Capacitances.** The distributed capacitance of the metallic carbon nanotubes was calculated according to Burke [1]—using a quantum capacitance of 0.1 nF/m and an electrostatic capacitance of 0.084 nF/m for a cylinder over a ground plane (in an infinite dielectric medium)—for a total capacitance of 0.8 aF for a 20 nm nanotube ($C_{ds}$). This capacitance is used as a parasitic between the source and drain to ground.

The gate capacitance calculation followed the derivation set forth by Guo et al. [8] for electrolyte-gated ($\kappa$ = 80) carbon nanotubes using a quantum capacitance of 0.4 nF/m and an electrostatic capacitance of 9 nF/m. This predicts a 7.6 aF gate capacitance for semiconducting carbon nanotubes 20 nm in length ($C_g$).

**Inductances.** The kinetic inductance described by Burke [1] for a metallic carbon nanotube is 0.32 nH for a nanotube length of 20 nm ($L_{ds}$, $L_g$). As described, the kinetic inductance dominates the vanishing magnetic inductance as the nanotube diameter approaches zero.

**Putting It All Together.** For a p-type FET, we end up with the circuit model illustrated in Figure 1a. Composing this p-type FET with a similarly constructed n-type FET leads us to the inverter circuit in Figure 1b. In general, we can continue to compose larger circuits and systems from these building blocks. Our CNFET models are pessimistic because they use over-estimates of the contact resistances as well as non-ballistic IV data from 1 to 3 micron long nanotubes [15] with mobilities that are orders of magnitude lower than those seen in the most recently observed back-gated devices [3]. The dearth of high-resolution (AC or DC) IV data available from some of these experiments makes modeling such devices with this method impractical.

## III. EXPERIMENTAL RESULTS

We now present the results of using our model to evaluate CNFET electronics and to compare against CMOS.

TABLE I
Switching time (ps) and Energy-delay ($10^{-24}$ J-s)

| Tech. | NAND | | FA (28T) | | SR-Latch | |
|---|---|---|---|---|---|---|
| | $t_d$ | ED | $t_d$ | ED | $t_d$ | ED |
| 180nm | 87.8 | 2.87 | 330 | 16.4 | 160 | 6.77 |
| 130nm | 76.5 | 0.612 | 280 | 3.16 | 130 | 1.24 |
| 100nm | 52.5 | 0.315 | 167 | 1.62 | 87.3 | 0.66 |
| 65nm | 57 | 0.268 | 169 | 1.27 | 92 | 0.52 |
| 45nm | 54 | 0.140 | 161 | 0.789 | 89.1 | 0.29 |
| CNFET | 10.3 | $4 \times 10^{-4}$ | 16.7 | $2 \times 10^{-3}$ | 14.4 | $7 \times 10^{-4}$ |
| 18nm | 2.81 | 0.018 | - | - | - | - |

### A. Methodology

We have developed a custom SPICE kernel based on the SPICE 3f5 source [5, 4]. This semi-empirical method enables the use of empirical device data (linearly interpolated) with analytical device models without relying on parameter fitting and assumptions about fundamental device operation.

The CNFET models we have developed are validated by simulating typical experiments performed by device physicists to characterize CNFETs, including the experiments

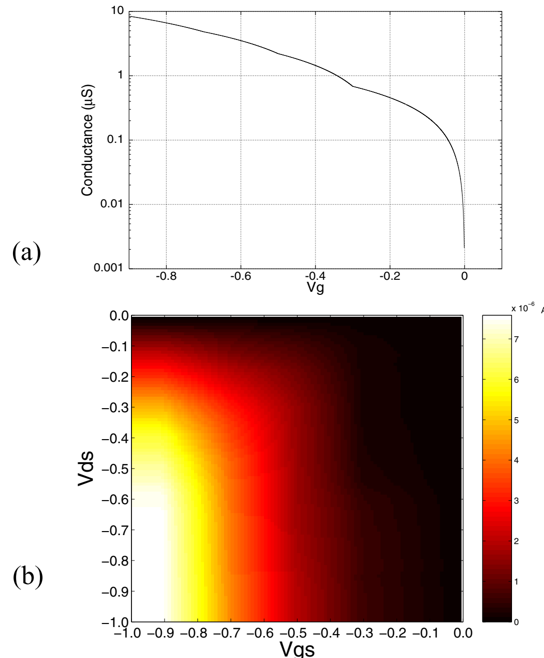


Fig. 2. (a) Conductance versus gate voltage and (b) the $I_{ds}$ current surface for the p-type CNFET.

performed on the original device. Our model demonstrates a maximum $I_{ds}$ current of 8.3 $\mu A$ ($\phi$ = 3 nm, or 1.17 $A/\mu m^2$), and transconductance of 18 $\mu A/V$, which are in good agreement with the reported values [15].

In our experiments, switching delay ($t_d$) and energy are measured for a single circuit with FO-4 loading ($W_n = 4\lambda$, $W_p = 8\lambda$). Square wave input signals pass through four inverters for conditioning. Each reported measurement is the worst-case delay or energy consumption over all single input transitions.

### B. *Results*

Figure 2a illustrates the conductance versus gate voltage for our p-type model. Our simulated devices have subthreshold swings of 73±47 mV/decade which is consistent with the reference data. Figure 2b illustrates the current versus gate and drain voltage relationship. This closely resembles the original device data over our operating range. In Table I, we show the performance and energy-delay results for the CNFETs and CMOS. We see that CNFETs outperform all CMOS nodes except for the predicted 18nm[1] and that their energy-delay product is far less than all CMOS nodes. The energy savings of CNFETs reflects the small capacitances on the nanotubes, despite their large resistances and inductances. CMOS performance plateaus below 100nm, although energy-delay continues to improve. This effect is due in part to maintaining the same transistor sizing ratios for all technologies, in order to make fair comparisons.

## IV. Conclusions

To compare carbon nanotube field effect transistors against current and future silicon CMOS technologies, we have developed a semi-empirical SPICE model of CNFET nanoelectronics. Our experiments show that, even with pessimistic assumptions, CNFET nanoelectronics can achieve significantly greater performance than predictive CMOS models foreshadow at a fraction of the switching energy.

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1. The 18nm data is shaded because it is past the ITRS's "red brick wall." The ITRS has not yet published 18nm data for full adders or SR-latches.