

Quantitative analysis of individual metal-CdSe-metal nanowire field-effect transistors

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Heterostructured metal-CdSe-metal nanowires were fabricated by sequential electrochemical deposition of layers of Au and the semiconductor CdSe. Nonlinear I - V curves were observed, and a parameter retrieval model was used to extract the majority carrier mobility of $0.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for nanowires fabricated with zero deposition current during the exchange of the final CdSe and Au segments. This improved threefold with the application of a small current during the solution exchange. Values for the resistance and the electron density for these nanowires were determined.

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Quasi-one-dimensional semiconductor materials such as nanotubes and nanowires have been studied in recent years due to their interesting optical properties^{1,2} as well as their potential for use in applications requiring active electrical components for computer circuitry. Cadmium selenide (CdSe) has received significant attention as a direct bandgap material with good optoelectronic properties and excellent stability in wet photovoltaic cells.³ Nanostructures of various shapes and sizes with different functionalities have been constructed, which include test beds for exploring quantum confinement,⁴ multicolor lumiphores,⁵ multishell nanocrystals,⁶ and quantum dots that exhibit stability over a wide range of pH values and ionic strengths.⁷ Fabrication methods used to produce these structures include aqueous and organic solution routes,⁸ molecular beam epitaxy,⁹ template methods with photochemical synthesis,¹⁰ and electrochemical deposition.^{11,12}

Template based methods for nanowire fabrication are particularly attractive due to low costs and ease of control over the dimensions of the nanowire. Klein *et al.* produced arrays of cadmium chalcogenide nanowire arrays and probed the I - V response of the entire array.¹³ Pena *et al.*¹¹ and Kovtyukhova *et al.*¹² have also constructed nanowires in porous alumina (PA) templates with well defined diameters and lengths. Their investigations on electrical transport through CdS and CdSe nanowires addressed the effects of photoelectric induced I - V changes and a coaxial SiO_2 gate dielectric.

This report examines how the introduction of a graded interface between the metal and semiconductor region affects the majority carrier mobility of heterostructured metal-semiconductor-metal nanowires. A parameter retrieval method is applied to determine the electrical transport characteristics of heterostructured fabricated by the electrochemical reduction of metal and semiconductor ions from solution into PA templates. The nanowires are released and deposited onto optically patterned substrates and are then wired to large metal pads through electron beam lithography. The doped Si/SiO_2 substrate acts as a backgate that modulates

the conductance of individually addressed nanowires.

PA templates were prepared by the thermal evaporation of Ag onto one side of the template and CdSe nanowires were fabricated electrochemically¹¹ as a segment of stoichiometric CdSe sandwiched between two or more metallic segments. A commercial potentiostat (PST050, Radiometer Analytical) was used for the reduction of metal from solution into the PA template and was placed into a homemade cell and connected as the working electrode along with a Pt counterelectrode and a Ag/AgCl (saturated KCl) reference electrode. The nanowires were then released from the template via immersion in a $3M$ NaOH solution for 30 min. The remaining particulate matter was separated from the nanowires by repeated rinsing with a combination of ethanol and distilled water, followed by centrifugation.

Macroscopic leads were fabricated on p^+ - Si/SiO_2 substrates with photolithography and nanowires were deposited from an ethanol/ dH_2O suspension onto the substrates. Ti:Au electrical contacts were written from the optical contact pads to the nanowires via electron beam lithography.¹⁴ All electrical measurements were recorded in ambient conditions at room temperature with a Keithley 2400 sourcemeter and custom National Instruments LABVIEW code.

Figure 1 depicts the typical physical characteristics of the heterostructured nanowires. The nanowires have mean

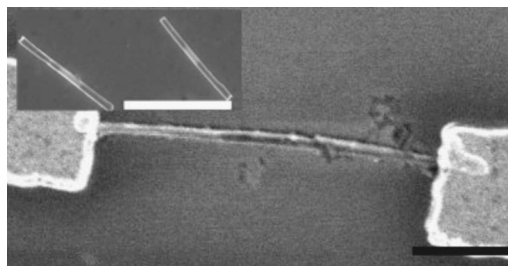


FIG. 1. Scanning electron microscopy (SEM) image of a FET based on a heterostructured Au-CdSe-Au nanowire, 80 nm in diameter. The darker section near the middle of the nanowire is composed of CdSe. Scale bar is 1 μm . The inset contains a SEM of identically structured nanowires with diameters of 200 nm. Scale bar is 5 μm .

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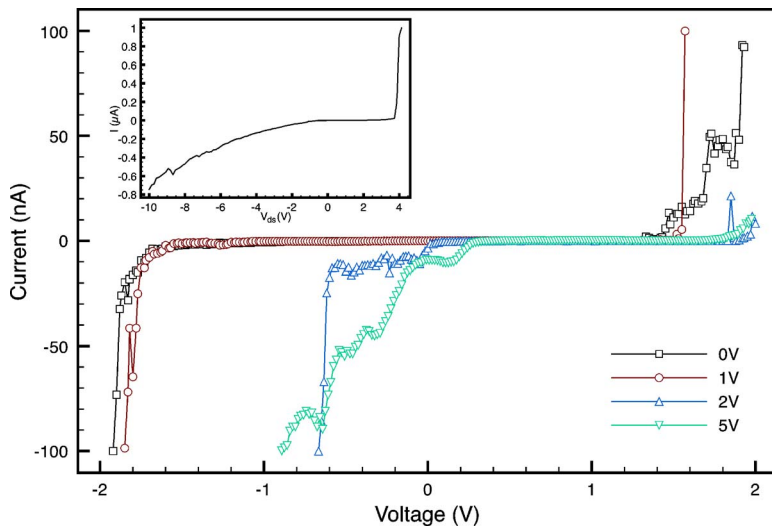


FIG. 2. (Color online) Small bias I - V response of 200 nm heterostructured Au-CdSe-Au nanowires as a function of applied backgate. Inset experimental I - V curves typical of heterostructured nanowires 80 nm in diameter.

lengths of $4.0 \pm 0.22 \mu\text{m}$ and an average CdSe channel length of $1.1 \mu\text{m} \pm 0.09 \text{ nm}$, which can be altered by varying the number of cycles performed during the CdSe electrodeposition step. The mean diameter of the nanostructures is $80 \pm 7 \text{ nm}$, as is determined by the PA template.

Electrical characteristics are retrieved by using the model of Zhang *et al.*¹⁵ Thermionic emission is the most commonly used model for Schottky contacts and is, thus, often used when analyzing the forward-biased current of semiconductor nanowires.¹⁶ The reverse-biased current, however, is underestimated,¹⁷ and although this is negligible for microelectronic structures where the saturation current occurs at relatively low bias, it becomes non-negligible for nanoelectronic devices since the device current is much smaller (10 nA). Here, the analysis carried out makes use of a model based on the thermionic field emission model of theory formulated by Padovani and Stratton¹⁸ that accounts for the tunneling effects of a reverse-biased junction, which dominates the reverse-biased current and explains the almost symmetric I - V curves.

Figure 2 contains typical experimental I - V curves from 200 and 80 nm diameter heterostructured nanowires. The resistance obtained at high bias¹⁶ is $R = a_{\text{NW}}(dV/dI) \approx dV/dI = 1.4 \pm 0.3 \text{ M}\Omega \text{ cm}^{-1}$, where a_{NW} is the voltage drop factor

of the reverse biased Schottky barrier. Near zero bias, the resistances are much larger ($>10 \text{ G}\Omega$).

We then focus on the intermediate biased regime of the I - V curve and apply

$$\ln I = \ln(SJ) = \ln(S) + V \left(\frac{q}{kT} - \frac{1}{E_0} \right) + \ln J_s, \quad (1)$$

where S is the contact area of the Schottky barrier, J is the current density through this barrier, E_0 is a parameter that depends on the density of the majority carriers, and J_s is a slowly varying parameter based on the applied bias.¹⁷ Figure 3 contains the logarithm of the current in this intermediate regime versus the source-drain voltage, which yields a straight line with slope $q/(kT) - 1/E_0$. This slope leads to E_0 of 47 meV and can be used to find the characteristic energy E_{00} (Ref. 19) obtained from $E_0 = E_{00} \coth(qE_{00}/kT)$, with

$$E_{00} = \frac{qh}{4\pi} \left[\frac{N_d}{m^* \epsilon_s \epsilon_0} \right]^{1/2}. \quad (2)$$

The electron concentration N_d can be extracted from Eq. (2) and the electron mobility can be calculated from $\mu = 1/qn\rho$, where ρ is the resistivity of the heterostructured nanowire and $n = N_d$. Combining this information, we obtain a value of $1.5 \pm 0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for nanowires constructed

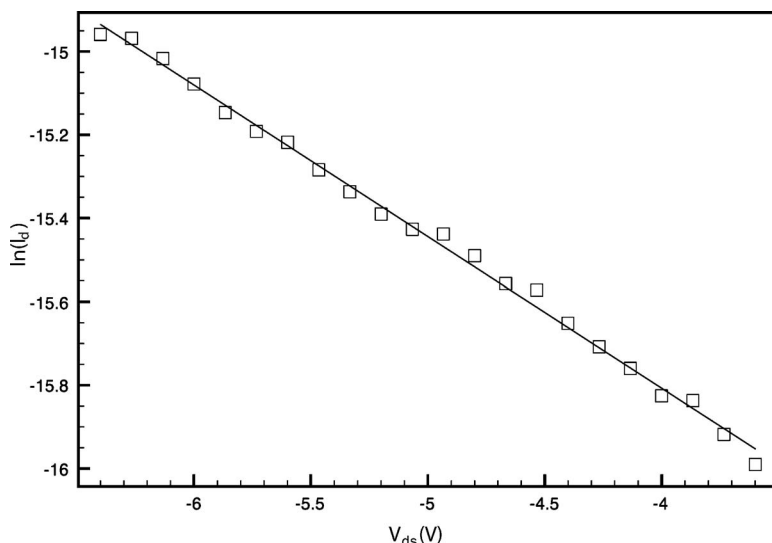


FIG. 3. $\ln(I)$ vs V plots (circles: experiment and line: model) from Fig. 2 of heterostructured nanowires at intermediate bias.

with a current of 0.03 mA/cm^2 applied during the exchange of the semiconductor and metal electrolytes. This value is significantly greater than the $0.5 \pm .03 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ from nanowires using an identical fabrication recipe but with zero current applied as the solution was exchanged.

The electron mobility μ of a nanowire is typically calculated via the transconductance g_m for a given source-drain bias²⁰ via $\mu = g_m L^2 / CV_{sd}$, where C can be estimated as the capacitance for a cylinder near an infinite plane $C = 2\pi\epsilon L / \ln(2t/r)$, ϵ is the dielectric constant of the SiO_2 , L is the channel length of the nanowire, t is the thickness of the oxide layer, and r is the radius of the nanowire. We find $\mu = 0.49 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is significantly less than the value derived above. The main difficulty with the infinite plane model is that our gate oxide does not fill the entire space surrounding the nanowire. This contradiction results in an overestimation of the capacitance and a decrease in the inferred mobility.²¹

The heterostructured nanowire field-effect transistors (FETs) yielded transconductances of $\sim 20 \text{ nS}$ for V_{sd} of 1.0 V . The normalized transconductance (g_m/W) was $\sim 100 \text{ nS}/\mu\text{m}$ [channel width (W) = 200 nm] and is over an order of magnitude higher than those found in structures such as ZnO nanobelts,²² but are an order of magnitude less than high quality single-crystal ZnO FETs fabricated via catalyst-free metal organic vapor phase epitaxy which may find use in applications for high-speed electronics.²³ For comparison, mobilities in Si metal-oxide semiconductor FETs with a 10 nm channel width have been reported to be between 10 and $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is considerably lower than the values for bulk silicon^{24,25} and as such, the lower mobilities here are not to be unexpected.

Zhang *et al.* noted that an interfacial insulating layer between material interfaces may affect the tunneling current at very low bias.¹⁷ For the nanowires fabricated here, any effects from an insulating layer between the metallic and semiconducting portions of the nanowire are minimal as the contacts are defined *in situ* during the construction of the nanowire itself. We note that the dependence on the current as electrochemical solutions were exchanged may indicate that a graded interface formed by dithering the Au and CdSe materials to create a Au-doped CdSe region would be helpful in achieving the highest currents, not unlike methods previously used in the creation of quantum cascade lasers con-

structed by metal organic vapor phase epitaxy.²⁶

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