

Performance Simulation of Nanoscale Silicon Rod Field-Effect Transistor Logic

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Abstract — We have simulated the behavior of a rod shaped nanoscale ring-gated field-effect transistor (RG-FET) using the PISCES-IIb[1] semiconductor drift-diffusion solver. The results from these simulations are used by a customized SPICE 3f5[2] kernel to simulate several simple logic gates. The usefulness of this kind of transistor is examined within the context of a self-assembling fabrication technique that we outline. Our simulation results, SPICE kernel modifications, and input decks may be found at ftp://ftp.cs.unc.edu/pub/packages/GRIP/publication_addenda/TSNSRFET.

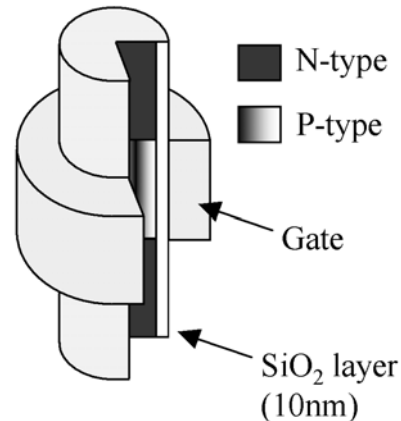


Fig. 1. N-type RG-FET. The rod length is 500nm and its radius is 50nm. Channel length is 150nm. All contacts are palladium ($\phi_m \approx 5.0$ eV)

I. INTRODUCTION

Recent advances in nanoscience enable new possibilities for nanoscale computer architecture. It is widely speculated that through the controlled placement and composition of these nanomaterials the landscape of modern computing will be changed. The self-assembly of nanomaterials by DNA hybridization is a breakthrough that appears to have promise in building ordered nanoscale 3D circuit structures [3]. This type of process can assemble nanoscale rods into organized surfaces and may be able to assemble more complex 3D rod lattices.

The RG-FET we have simulated (fig. 1) is similar in structure to the surrounding-gate transistors (SGTs) that have been studied for more than a decade as high-density alternatives to planar transistors [4-7]. The RG-FET is novel because of the nature of its fabrication and placement within a self-assembling device structure. The RG-FET can be incorporated into a DNA-guided self-assembly process by chemically attaching different DNA strands to each end of the rod during the rod's formation, in a fashion analogous to that in [8]. Nano-porous alumina synthesis of silicon nanorods [9] is particularly attractive because it provides many ways to control the attachment of the DNA to each end of the rod. Other methods have been used to synthesize doped silicon rods [10] but these

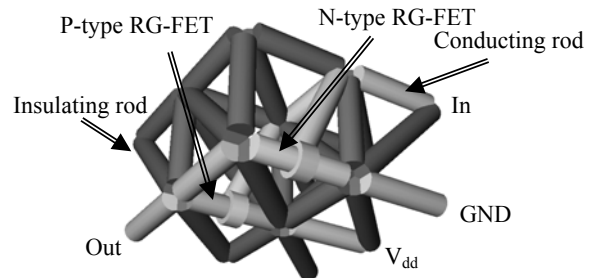


Fig. 2. RG-FET inverter. Insulating and conducting rods are used for support.

methods grow rods from nucleating particles on surfaces. Such methods may not have the necessary control over where the DNA strands attach.

Fig. 2 illustrates a simple CMOS inverter in the shape of a 3D rod lattice. The junctions between rods are metallized DNA strands that have low ohmic resistances [11]. This type of self-assembled 3D structure could have as many as 10^{19} components. Such large numbers of devices would require communication buses with hundreds of thousands of bit lines and access rates of gigahertz to enumerate all devices in 24 hours. A machine as large as this may seem unusable, but when

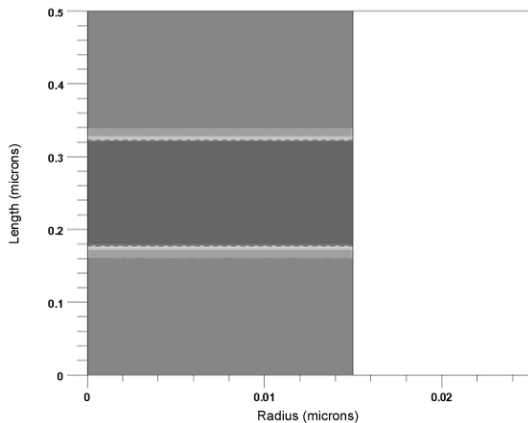


Fig. 3. RG-FET doping profile along radius of rod (not to scale). Oxide layer on right. PNP or NPN layers on left side.

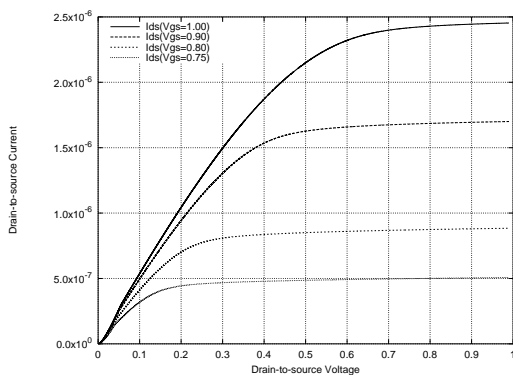


Fig. 4. N-Type RG-FET IV curves.

coupled with a parallel search technique can open up large problem spaces that have been conventionally inaccessible.

The importance of low power digital circuitry to conventional devices is well known and will become even greater as both transistor density and clock rates increase. Molecular scale electronic devices will therefore require either ultra low power consumption gates or slow clock rates, and perhaps both if they are to consume less than kilowatts of power. Thus, the need for low power logic circuitry becomes an important issue to molecular scale device design.

II. PISCES-IIb RG-FET SIMULATION RESULTS

The size scale of the RG-FET silicon rod we consider (50 nm diameter, 500 nm length) is large enough to use classical drift-diffusion simulations

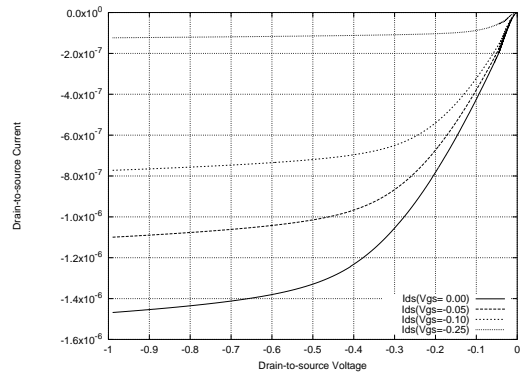


Fig. 5. P-Type RG-FET IV curves

[12] which makes this type of mixed-mode simulation (drift-diffusion with transistor-level simulation) less computationally intensive than other, more sophisticated methods developed to handle smaller sized junctions accurately. Drift-diffusion simulations were performed using a Win32 port of PISCES-IIb.[1] The geometry of the RG-FET is depicted in fig. 1. Using cylindrical symmetry PISCES-IIb was able to simulate the structure in 3D.

The doping profile used by PISCES-IIb is shown in fig. 3. The substrate (a silicon rod in this case) was doped to 1×10^{15} p-type atoms/cm³ with the ends doped to 1×10^{21} n-type atoms/cm³ for the n-type RG-FET. The p-type RG-FET was doped to 1×10^{18} n-type atoms/cm³ with the ends doped to 1×10^{22} p-type atoms/cm³. Each FET was doped using a Gaussian profile with n-type and p-type characteristic lengths of 0.0475 μ m and 0.061 μ m respectively.

We performed a time independent simulation by applying a V_{ds} bias across the device (top to bottom) and a V_{gs} bias between the oxide side (right) and the bottom electrode. The simulation model included Shockley-Read-Hall recombination with concentration-dependent lifetimes as well as concentration and lateral field-dependent mobility. Boltzmann statistics were used throughout with an operating temperature of 300K. To capture the time independent behavior of the RG-FET we swept V_{gs} and V_{ds} from 0.0v to ± 1.0 v (-1.0v for the p-FET and 1.0v for the n-FET). Each step was 0.5mV and 1mV steps along V_{gs} and V_{ds} , respectively, and I_{ds} recorded (current from top to bottom) to form the IV-curves in figures 4 and 5. The simulated transconductances

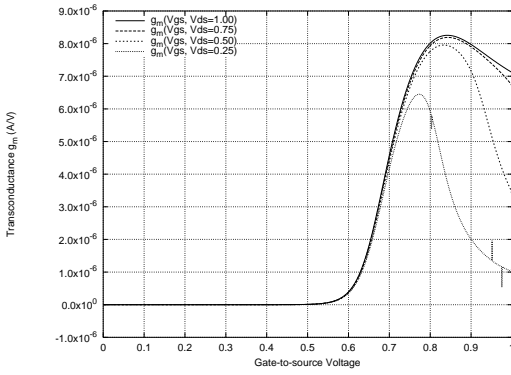


Fig. 6. N-Type RG-FET transconductance at several source-drain voltages. The glitches in the $V_{ds}=0.25$ transconductance trace are a computational artifact due to the low drain-to-source voltage.

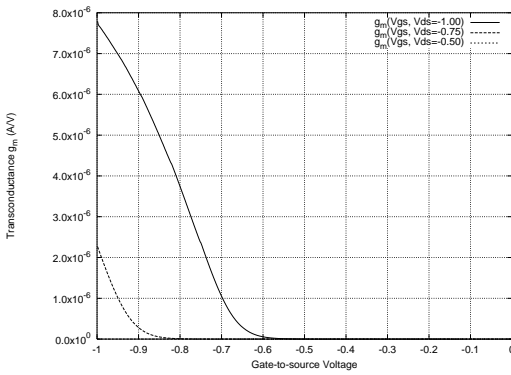


Fig. 7. P-Type RG-FET transconductance at several source-drain voltages.

of the n-type and p-type RG-FETs are plotted in figures 6 and 7 respectively.

The data illustrated in figures 4 and 5 were stored on disk for later use by our modified SPICE 3f5 kernel. Our method of mixed-mode simulator coupling is similar to that used in [13]. Instead of using an inner Newton iteration we simply preprocess the analog response of the RG-FET for later use by SPICE.

III. SPICE 3F5 SIMULATION RESULTS

A modified SPICE 3f5 circuit simulator kernel was used to simulate the behavior of several RG-FET logic devices. Our only kernel modification was to include a simple file-based table lookup feature for the arbitrary current or voltage source device. The file-based table lookup was used to read current data from the PISCES-IIb output files.

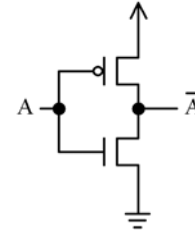


Fig. 8. An inverter.

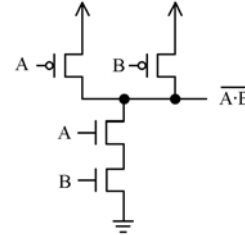


Fig. 9. Two input NAND gate.

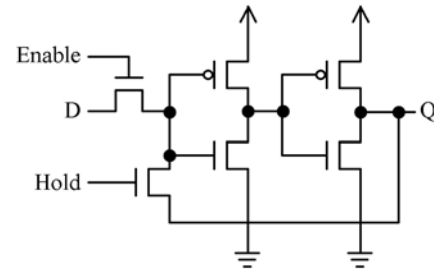


Fig. 10. A level-sensitive D-latch. De-asserting “hold” is used to break the feedback when asserting a new data value. See fig. 15 for signaling details.

The data is loaded into a memory table by the SPICE kernel and current values (I_{ds}) are linearly interpolated between V_{gs} and V_{ds} data points.

We have simulated an inverter, a 2-input NAND gate, and a D-latch as illustrated in figures 8, 9, and 10. The purpose of these simulations is to estimate the power consumption of typical logic cells fabricated using RG-FETs. Since power consumption estimates require accurately modeled parasitic capacitances, we have included lumped capacitances at every node of each RG-FET as illustrated in fig. 11. The values for the parasitic capacitances were derived from a boundary element method solution to the electrostatic field problem (COULOMB) for a conducting rod surrounded by grounded rods as shown in figure 12[14].

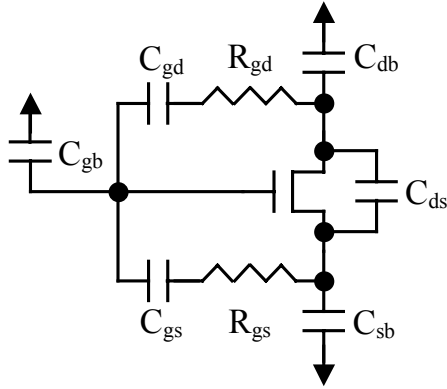


Fig. 11. Node capacitance circuit model.

The COULOMB simulation results reported a capacitance of 1.71×10^{-17} F between the center rod in figure 12 and the surrounding shell of rods. COULOMB also reported the capacitance between two parallel and adjacent rods to be 1×10^{-19} F. The values of R_{gs} and R_{gd} were estimated using the calculated resistance of a 10 nm thick silicon dioxide disk. Using the value of the simulated “cage” capacitance for C_{gb} , C_{sb} , and C_{db} and the adjacent rod capacitance for C_{gs} , C_{gd} , and C_{ds} , we simulated several test cases. Figures 13, 14, and 15 depict the results of our simulations. Table I lists the gate delays, power consumption, and power-delay products (PT).

Table I

Gate	Delay (ns)	Power (nW)	PT-product (J)
NOT ¹	0.6	0.59	3.54×10^{-19}
RG-FET NAND2 ¹	0.75	0.69	5.175×10^{-19}
CMOS NAND2 ²	3.2	1300	4.16×10^{-15}
D-latch ¹	0.65	3.8	2.47×10^{-18}

¹ Input slew rate of 0.2 V/ns. Unloaded output. See figs. 13, 14, and 15.

² 1.5V 0.6 μ m CMOS comparison from [14].

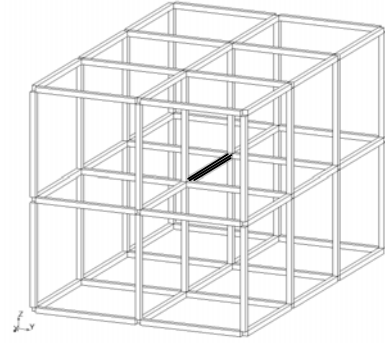


Fig. 12. Rod geometry for parasitic capacitance calculation. The capacitance is measured between the center rod (shaded) and the outer shell of rods.

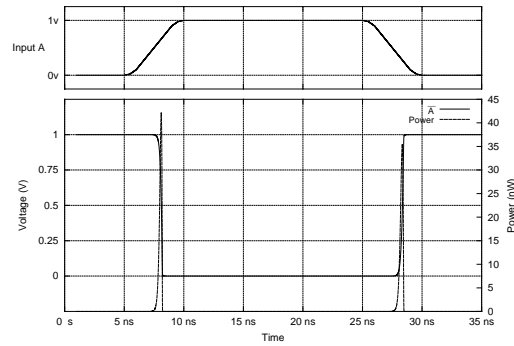


Fig. 13. Inverter input, output, and power consumption. Mean power-delay product per transition is 3.54×10^{-19} J.

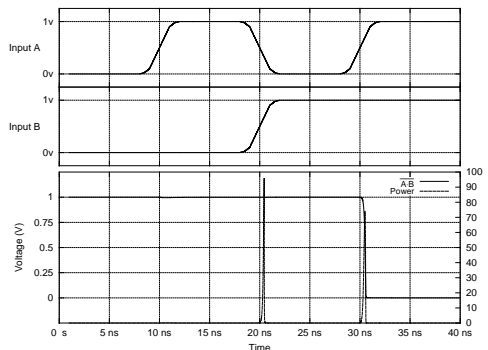


Fig. 14. NAND input, output, and power consumption. Mean power-delay product per transition is 5.175×10^{-19} J.

IV. DISCUSSION

We have observed a reduction of approximately four orders of magnitude in the power-delay product between the comparison and RG-FET NAND gate. The comparison NAND gate from [15] was simulated using an HSPICE FET model at 1.5V with a 50 fF output load. The RG-FET

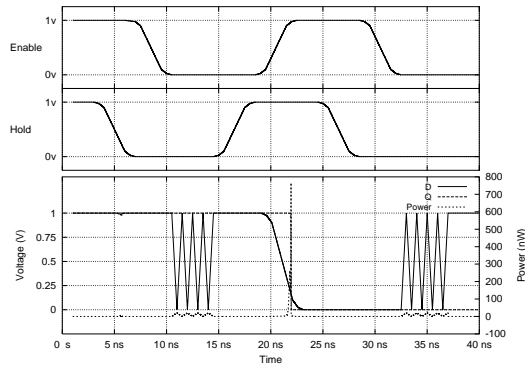


Fig. 15. D-latch input, output, and power consumption. Mean power-delay product per transition is 2.47×10^{-18} J. The input signal D is oscillated to show that the latch is opaque.

NAND gate (and other gates) were simulated using 1.7×10^{-17} F output loads. We have no reason to expect that the derivation of dynamic CMOS power consumption will change from typical VLSI technology to this technology, namely the formula $P = V_{dd}^2 \cdot C_L \cdot f_c$ will still hold. The three orders of magnitude difference between the comparison gate output load and the RG-FET gate can explain a large portion of the power-delay reduction. This advantage comes from the small substrate/body capacitance of the RG-FET because they are relatively isolated (thermally, as well) from the device structure. Low power consumption, as mentioned earlier, is even more important for this very reason. The loosely coupled RG-FETs are expected to have very long thermal cool-down periods compared with planar FETs. The additional factor of ten in power-delay product reduction (over the capacitive reduction) may come from differences in the drive characteristics of the FETs used in [14] and the RG-FETs used here and may not represent any inherent design advantage.

The particular design decisions made before simulating the RG-FET logic gates were inspired from geometric and processing plausibility arguments starting from a 1V process with 500 nm long rods that are 50 nm in diameter. As figure 1 illustrates, the RG-FET cannot accommodate oxide thicknesses much greater than about 20 nm. Similarly, oxides thicker than 20 nm will reduce the channel diameter below the limit of continuum transport mechanisms [12]. Oxides less than 5 nm thick will require extremely precise control of the oxide growth to ensure a highly uniform and strong

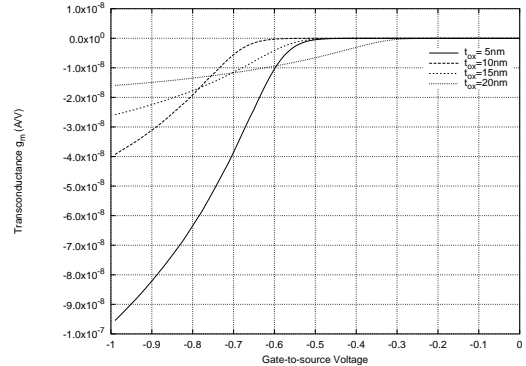


Fig. 16. P-type RG-FET transconductance as a function of oxide thickness. We used the 10nm thick oxide RG-FET in our performance evaluations.

crystal. The quality of the oxide is important in preventing breakdown of the film at gate voltages of approximately 1V. Therefore, we chose an oxide thickness of 10 nm because it can withstand the electric fields developed at a gate voltage of 1V. Figure 16 illustrates the change in transconductance as oxide thickness is varied from 5 nm to 20 nm.

Expected processing limitations in the fabrication of an RG-FET motivated our choice of a 150 nm long channel. The lengthwise etch of the RG-FETs channel region may not be precisely controllable. Therefore, a sufficiently large margin (channel extension) must be left on either side of the channel. Channel lengths greater than 200 nm leave only 150 nm of rod on either side of a 500 nm long rod. Channel lengths below 75 nm will experience poor off-state leakage currents [16] and may not be properly simulated by PISCES-IIb. Figure 17 illustrates the change in transconductance as the channel length is varied.

The input slew rates used in our simulations (0.2 V/ns) lead to conservative power estimates because they prolong the overlapping n-type and p-type RG-FET transition period with respect to the output transition time thus increasing the switching energy. The output transition times are consistent with the turn-on time observed in a time dependent PISCES-IIb simulation of a p-type RG-FET. The time dependent simulations also show that the gate charging current due to the voltage dependent channel capacitance is instantaneously never greater than 1 nA for 0.2 V/ns input slew rates (it drops to zero as the slew rate goes to zero).

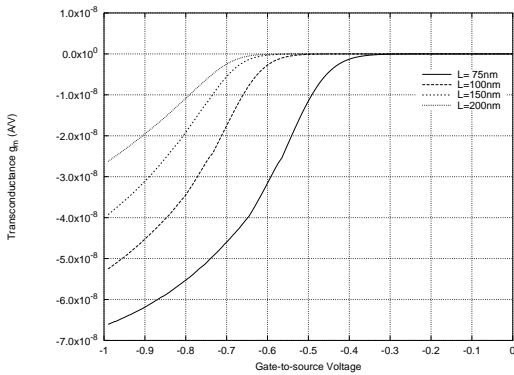


Fig. 17. P-type RG-FET transconductance as a function of channel length. We used the 150nm channel length RG-FET in our performance evaluations.

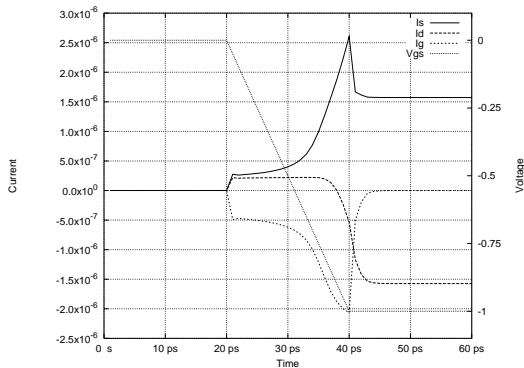


Fig. 18. Transient response of a p-type RG-FET during a 20ps input voltage ramp.

We have performed additional transient response simulations to clarify the error that we incur by using a DC approximation to the RG-FETs transfer function. We measured the time varying current response (I_{ds} vs. time) using several different slew rates (1 V/ms, 0.4 V/ μ s, 0.8 V/ μ s, 1.5 V/ns, 3 V/ns, 6 V/ns, 12.5 V/ns, 25 V/ns, and 50 V/ns). Figure 18 is a representative result from the transient simulations. The positive source and drain currents counter the displacement current seen in the gate. This is presumably due to the movement of charges as the channel forms underneath the gate. To compare the DC response with the different transient responses we plot the log of the absolute difference between the currents versus time. Figure 19 illustrates several of these error curves. The errors we observe during the 3V/ns slew rate simulation can be as low as a few hundred electron/holes per second. This current is smaller than what can typically be simulated by the PISCES-IIb simulator. This implies our DC method is as accurate as a transient simulation

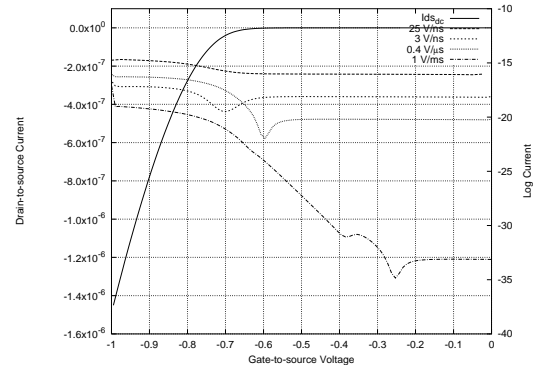


Fig. 19. Absolute current error between DC and transient p-type RG-FET response.

using PISCES-IIb for input slew rates less than 3 V/ns.

V. SUMMARY

We have presented the results from a semiconductor carrier mobility simulation (PISCES-IIb) for a nanoscale ring gated field effect transistor we call the RG-FET. We have also presented the SPICE simulation results of several logic circuits constructed from this type of transistor. These results indicate that the loosely coupled RG-FET structures can reduce the power-delay product of CMOS circuitry by as much as four orders of magnitude. We have also analyzed the error that results from using a DC response for the RG-FET versus a transient response and found that for slew rates below 3 V/ns the absolute difference between the two is less than 1×10^{-17} A. The low power consumption and nanoscale size of such logic circuits make them particularly interesting to nanoscale process designers as potential targets for future work. Our future work will focus on how to apply such nanoscale circuitry to solve large-scale nonlinear optimization problems.

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