

# Transport Simulation of a Nanoscale Silicon Rod Field-Effect Transistor

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**Abstract** — We have simulated the behavior of a rod shaped nanoscale ring-gated field-effect transistor (O-FET) using the PISCES-IIb[1] semiconductor drift-diffusion solver. The results from these simulations are used by a custom SPICE 3f5[2] kernel to simulate several simple logic gates. The usefulness of this kind of transistor is examined within the context of a self-assembling fabrication technique that we outline. We also briefly explore a computer architecture we call a “computational oracle” for which the O-FET is well suited. Our simulation results, SPICE kernel modifications, and input decks may be found at [ftp://ftp.cs.unc.edu/pub/packages/GRIP/publication\\_addenda/TNSRFET](ftp://ftp.cs.unc.edu/pub/packages/GRIP/publication_addenda/TNSRFET).

## I. INTRODUCTION

Recent advances in nanoscience enable new possibilities for nanoscale computer architecture. It is widely speculated that through the controlled placement and composition of these nanomaterials the landscape of modern computing will be changed. The self-assembly of

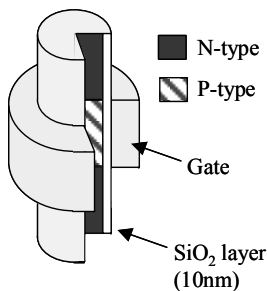


Fig. 1. N-type O-FET. The rod length is 500nm and its radius is 50nm. Channel length is 150nm. All contacts are palladium ( $\phi_m \approx 5.0$  eV)

nanomaterials by DNA hybridization is a breakthrough that appears to have promise in building ordered nanoscale 3D circuit structures.[7] This type of process can assemble nanoscale rods into organized surfaces and may be able to assemble more complex 3D rod lattices. The O-FET (fig. 1) can be incorporated into such a DNA-guided self-assembly process by chemically attaching different DNA strands to each end of the rod during the rod's formation. Nano-porous alumina synthesis of silicon nanorods [5] is particularly attractive because it provides

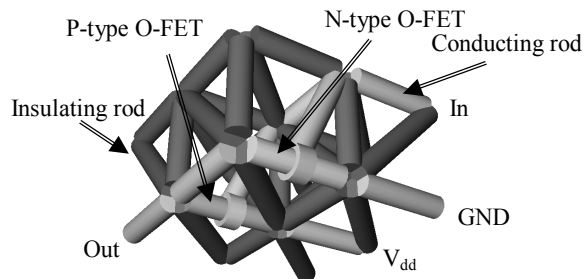


Fig. 2. O-FET inverter. Insulating and conducting rods are used for support.

many ways to control the attachment of the DNA to each end of the rod. Other methods have been used to synthesize doped silicon rods [6] but these methods grow rods from nucleating particles on surfaces. Such methods may not have the necessary control over where the DNA strands attach.

Fig. 2 illustrates a simple CMOS inverter in the shape of a 3D rod lattice. The junctions between rods are metallized DNA strands that have low ohmic resistances.[8] This type of self-assembled 3D structure could have as many as  $10^{19}$  components. Such large numbers of devices would require communication buses with hundreds of thousands of bit lines and access rates of gigahertz to enumerate all devices in 24 hours. A machine as large as this may seem unusable but, when coupled with a parallel search technique, opens up large problem spaces that are conventionally inaccessible.

We propose a computing machine based on content addressable memories and distributed input spaces that we call a computational oracle. This class of machine rivals DNA-computing schemes in parallel computation yet realizes fast problem turn around times because it can be built using conventional digital circuitry. Our exploration of this architecture begins by examining the underlying electrical components of the fabrication technique starting with its transistors.

The importance of low power digital circuitry to conventional devices is well known and will become even greater as both transistor density and clock rates increase. Molecular scale electronic devices with on the order of

$10^{19}$  transistors will therefore require either ultra low power consumption gates or slow clock rates, and perhaps both if they are to consume less than a few kilowatts of power. Thus, the need for power conservative computer architectures becomes an important issue to molecular scale device design. The O-FET is well suited to such molecular scale fabrication schemes because it has limited dimensionality (axial symmetry with a ring gate) and good power consumption characteristics.

## II. PISCES-IIb O-FET SIMULATION RESULTS

Drift-diffusion simulations were performed using a Win32 port of PISCES-IIb.[1] The geometry of the O-FET is depicted in fig. 1. Using cylindrical symmetry PISCES-IIb was able to simulate the structure in 3D.

The doping profile used by PISCES-IIb is shown in fig. 3. The substrate (a silicon rod in this case) was doped to  $1 \times 10^{15}$  p-type atoms/cm<sup>3</sup> with the ends doped to  $1 \times 10^{21}$  n-type atoms/cm<sup>3</sup> for the n-type O-FET. The p-type O-FET was doped to  $1 \times 10^{18}$  n-type atoms/cm<sup>3</sup> with the ends doped to  $1 \times 10^{22}$  p-type atoms/cm<sup>3</sup>. Each FET was doped using a Gaussian profile with n-type and p-type characteristic lengths of  $0.0475 \mu\text{m}$  and  $0.061 \mu\text{m}$  respectively.

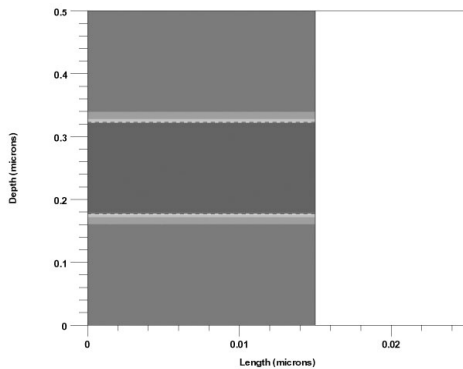


Fig. 3. O-FET doping profile along radius of rod (not to scale). Oxide layer on right. PNP or NPN layers on left side.

We performed a time independent simulation by applying a  $V_{ds}$  bias across the device (top to bottom) and a  $V_{gs}$  bias between the oxide side (right) and the bottom electrode. The simulation model included Shockley-Read-Hall recombination with concentration-dependent lifetimes as well as concentration and lateral field-dependent mobility. Boltzmann statistics were used throughout with an operating temperature of 300K. To capture the time independent behavior of the O-FET we swept  $V_{gs}$  and  $V_{ds}$  from 0.0v to  $\pm 1.0\text{v}$  ( $-1.0\text{v}$  for the p-FET and  $1.0\text{v}$  for the n-FET). Each step was  $0.5\text{mV}$  and  $1\text{mV}$  steps along  $V_{gs}$  and  $V_{ds}$ , respectively, and  $I_{ds}$  recorded

(current from top to bottom) to form the IV-curves in figures 4 and 5.

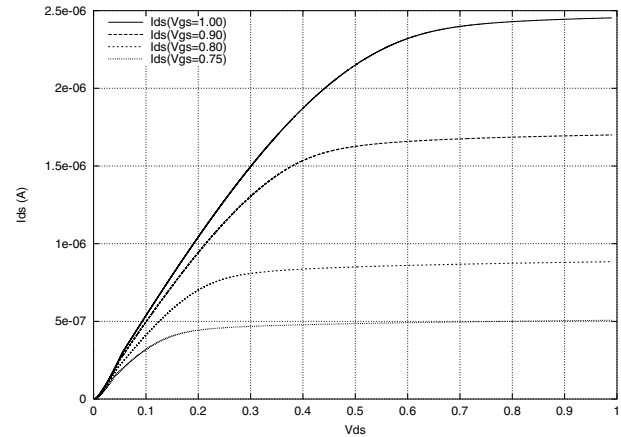


Fig. 4. N-Type O-FET IV curves

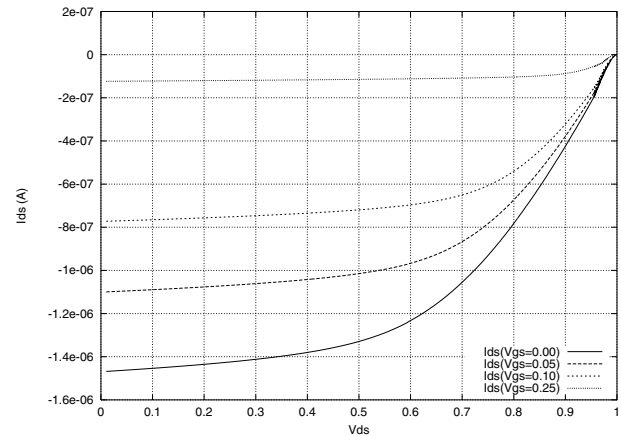


Fig. 5. P-Type O-FET IV curves

The simulated transconductances of the n-type and p-type O-FETs are plotted in figures 6 and 7 respectively.

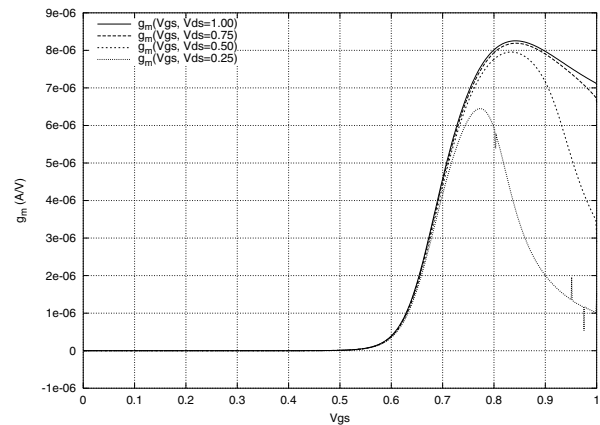


Fig. 6. N-Type O-FET Transconductance at several source-drain voltages.

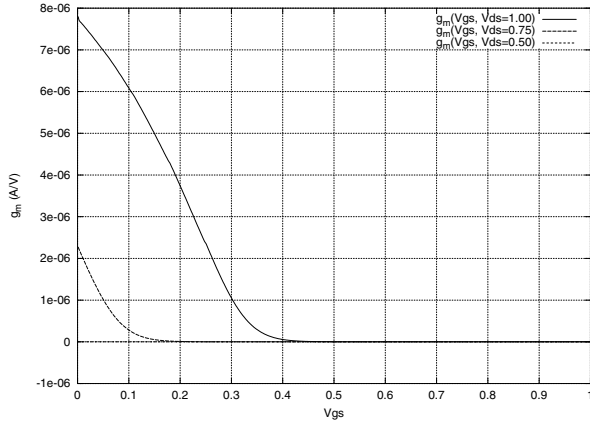


Fig. 7. P-Type O-FET Transconductance at several source-drain voltages.

The data illustrated in figures 3 and 4 were stored on disk for later use by our modified SPICE 3f5 kernel. Our method of mixed-mode simulator coupling is similar to that used in [3]. Instead of using an inner Newton iteration we simply preprocess the analog response of the O-FET for later use by SPICE.

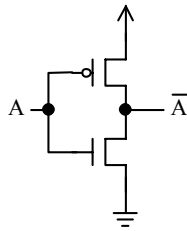


Fig. 8. An inverter.

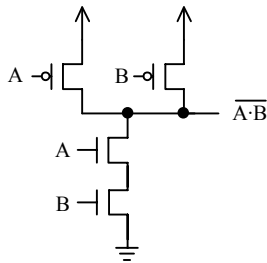


Fig. 9. Two input NAND gate.

### III. SPICE 3F5 SIMULATION RESULTS

A modified SPICE 3f5 circuit simulator kernel was used to simulate the behavior of several O-FET logic devices. Our only kernel modification was to include a simple file-based table lookup feature for the arbitrary current or voltage source device. The file-based table lookup was used to read current data from the PISCES-IIb output files. The data is loaded into a memory table by the SPICE

kernel and current values ( $I_{ds}$ ) are linearly interpolated between  $V_{gs}$  and  $V_{ds}$  data points.

We have simulated an inverter and a 2-input NAND gate as illustrated in figures 8 and 9. The purpose of these simulations is to estimate the power consumption of typical logic cells fabricated using O-FETs. Since power consumption estimates require accurately modeled parasitic capacitances, we have included lumped capacitances at every node of each O-FET as illustrated in fig. 10. The values for the parasitic capacitances were derived from a boundary element method solution to the electrostatic field problem (COULOMB) for a conducting rod surrounded by grounded rods as shown in fig. 11[4].

The COULOMB simulation results reported a capacitance of  $1.71 \times 10^{-17}$  F between the center rod in fig. 11 and the surrounding shell of rods. COULOMB also reported the capacitance between two parallel and adjacent rods to be  $1 \times 10^{-19}$  F. The values of  $R_{gs}$  and  $R_{gd}$  were estimated using the calculated resistance of a 10nm thick silicon dioxide disk. Using the value of the simulated

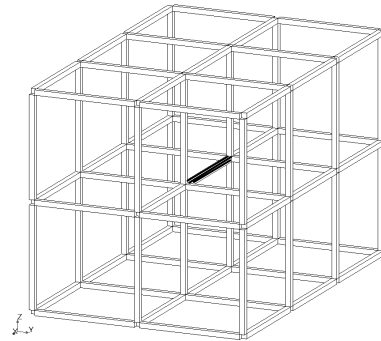


Fig. 11. Rod geometry for parasitic capacitance calculation. The capacitance is measured between the center rod (shaded) and the outer shell of rods.

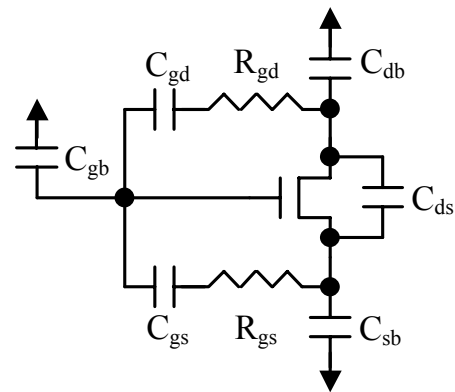


Fig. 10. Node capacitance circuit model.

“cage” capacitance for  $C_{gb}$ ,  $C_{sb}$ , and  $C_{db}$  and the adjacent rod capacitance for  $C_{gs}$ ,  $C_{gd}$ , and  $C_{ds}$ , we simulated

several test cases. Figures 12 and 13 depict the results of our simulations.

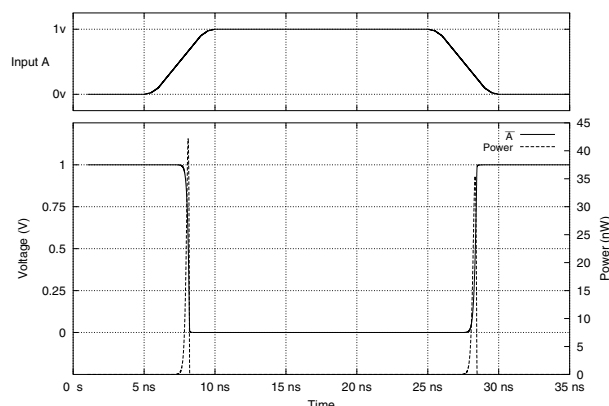


Fig. 12: Inverter input, output, and power consumption. Mean power consumption over entire simulation was 0.59 nW.

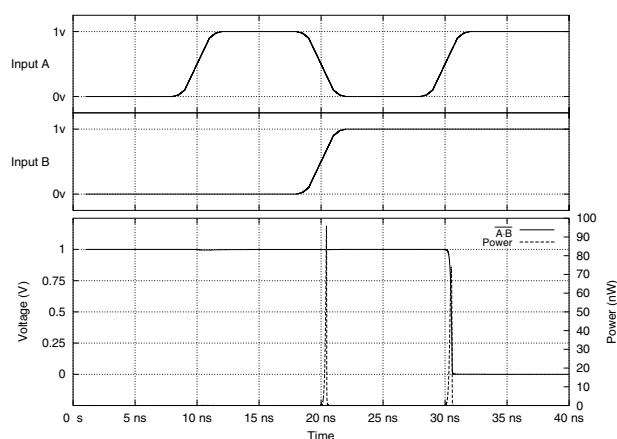


Fig. 13. NAND input, output, and power consumption. Mean power consumption over entire simulation was 0.69 nW.

The input slew rates used in our simulations lead to conservative power estimates because they prolong the overlapping n-type and p-type O-FET transition period with respect to the output transition time thus increasing the switching energy. The output transition times are consistent with the turn-on time observed in a time dependent PISCES-IIb simulation of a p-type O-FET. The time dependent simulation also showed that the gate charging current due to the voltage dependent channel capacitance is instantaneously never greater than 1 nA for 0.2 V/ns input slew rates (it drops to zero as the slew rate goes to zero).

#### IV. SUMMARY

We have presented the results from a semiconductor carrier mobility simulation (PISCES-IIb) for a nanoscale ring gated field effect transistor we call the O-FET. We have also presented the SPICE simulation results of several logic circuits constructed from this type of transistor. The low power consumption and nanoscale size of such logic circuits make them particularly interesting to nanoscale process designers as potential targets for future work. Our future work will focus on how to apply such nanoscale circuitry to solve large-scale nonlinear optimization problems.

#### ACKNOWLEDGMENTS

This work was supported by the NIH National Research Resource in Molecular Graphics and Microscopy at the University of North Carolina at Chapel Hill.

#### REFERENCES

- [1] M. R. Pinto, C. S. Rafferty, R. W. Dutton, M. J. Eldredge, Z. Yu, et al., PISCES-IIb 9009, Win32 port by J. Faricelli. See <http://www-tcad.stanford.edu/tcad/programs/ftpable.html>
- [2] T. Quarles, et al., SPICE3. See <http://bwrc.eecs.berkeley.edu/Classes/IcBook/SPICE>
- [3] Rollins, Gregory J. and John Choma, "Mixed-Mode PISCES-SPICE Coupled Circuit and Device Solver", *IEEE Transactions on Computer Aided Design*, vol. 7, no. 8, pp. 862-867, August 1988.
- [4] IES Inc., COULOMB, 2001. ([www.integratedsoft.com](http://www.integratedsoft.com))
- [5] B. R. Martin, D. J. Dermody, B. D. Reiss, F. Mingming, L. A. Lyon, M. J. Natan, T. E. Mallouk, "Orthogonal Self-Assembly on Colloidal Gold-Platinum Nanorods", *Adv. Mater.*, 11, no. 12, pp. 1021-5, 1999.
- [6] Y. Cui, D. Xiangfeng, J. Hu, C. M. Lieber, "Doping and Electrical Transport in Silicon Nanowires", *J. Phys. Chem.*, vol. 104, no. 22, pp.5213-6, June 8, 2000.
- [7] J. K. N. Mbindyo, B. D. Reiss, B. R. Martin, C. D. Keating, M. J. Natan, T. E. Mallouk, "DNA-Directed Assembly of Gold Nanowires on Complementary Surfaces", *Adv. Mater.*, 13, no. 4, pp. 249-54, February 19, 2001.
- [8] J. Richter, M. Mertig, W. Pompe, "Construction of highly conductive nanowires on a DNA template", *App. Phys. Lett.* vol. 78, no. 4, pp. 536-8, 2001.